



```

graph TD
    10[ACCUMULATOR] <--> 20[SATURATE]
    ENABLE --> 20
    20 --> 30[ADDER]
    40[OPERAND1] --> 30
    50[OPERAND2] --> 30

```

The diagram illustrates a 32-bit adder system. At the bottom, an **ADDER** (90) takes two inputs, **OPERAND<sub>1</sub>** and **OPERAND<sub>2</sub>**, and produces a 32-bit output **[b39:b0]**. This output is fed into a register (60) and also branches off to a logic block (20) enclosed in a dashed box. The register (60) has inputs **b39** through **b0** and is controlled by an **ENABLE** signal. The logic block (20) contains several AND gates (100, 105, 110, 115, 120, 125, 140, 145) and inverters (130, 135). It also receives a signal from the **OUT** of a multiplexer (95). The multiplexer (95) has inputs **A** and **B** and is controlled by a select line **I** (0 or 1). Input **A** is the output of the adder, and input **B** is a constant value **0x8000000000**. The output of the multiplexer is fed back into the register (60) and also branches off to the logic block (20). The logic block (20) produces a **TO OVERFLOW BIT** signal and a **TO SATURATION BIT** signal. The **TO SATURATION BIT** is the output of an OR gate (150) that combines the outputs of AND gates 140 and 145.